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Notice of Allowability	Application No.	Applicant(s)	
	09/944,472	HOWARTH, JAMES J.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/12/04*.

2. ☒ The allowed claim(s) is/are *1,4,6-9,11,13,20-24,27,30-33,35,36 and 43-46*.

3. ☒ The drawings filed on *02 September 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 11/12/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1 and 13 are generic and allowable. Accordingly, the restriction requirement as to the encompassed species is hereby withdrawn and claims 9 and 20-23, directed to the species of V, VI, VII and VIII no longer withdrawn from consideration since all of the claims to this species depend from or otherwise include each of the limitations of an allowed generic claim.

In view of the above noted withdrawal of the restriction requirement as to the linked species, applicant(s) are advised that if any claim(s) depending from or including all the limitations of the allowable generic linking claim(s) be presented in a continuation or divisional application, such claims may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 44 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Bradley Jensen (Reg. No. 46,801) on January 6, 2005.

The application has been amended as follows:

1. (Currently Amended) A method for aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween, the method comprising:

forming at least two channels through the semiconductor device package from a first major surface thereof to a second, opposing major surface thereof;

providing a major surface of the carrier substrate with at least two alignment features including forming at least two holes [[the]] in the carrier substrate, each of which are spaced and positioned in respective correspondence to one of the at least two channels;

~~forming at least one of the at least two pins with a mechanical self-locking mechanism proximate at least one end thereof;~~

~~carrying the at least two pins with a head of a pick and place device,~~ engaging the at least two channels formed in the semiconductor package with at least two pins carried by a head of pick and place device and grasping the semiconductor package with the pick and place device;

positioning the pick and place device and the semiconductor device package over the carrier substrate with the first major surface of the semiconductor package facing the major surface of the carrier substrate;

aligning the at least two pins with the at least two alignment features of the carrier substrate; ~~and~~

placing the at least two pins through the at least two channels and into the at least two holes; and

engaging a portion of a second, opposing surface of the carrier substrate with [[the]] a mechanical self-locking mechanism carried by at least one of the at least two pins.

24. (Currently Amended) A method of testing a semiconductor device package having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising:

providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements;

forming at least two channels in the semiconductor device package, each channel passing from a first surface thereof to a second, opposing surface thereof;

providing the carrier substrate with at least two alignment features including forming at least two holes the in the carrier substrate, each of which are respectively spaced and positioned in correspondence to one of the at least two channels;

placing the semiconductor device package over the carrier substrate;

aligning each channel of the at least two channels formed in the semiconductor device package with a corresponding alignment feature of the at least two alignment features of the carrier substrate including placing pins formed of a non-conductive material through the at least two channels and into the at least two holes;

electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality;

passing at least one electrical signal between the semiconductor device package and the carrier substrate; and

removing the pins subsequent to passing at least one electrical signal between the semiconductor device package and the carrier substrate ~~the alignment of each of the at least two channels with a corresponding alignment feature of the at least two alignment features~~.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

Claim 1 is allowed because the prior art does not teach the step of engaging a portion of a second, opposing surface of the carrier substrate with a mechanical self-locking mechanism carried by at least one of the at least two pins as instantly claimed, and in combination with the additional method steps.

Claim 13 is allowed because the prior art does not teach the step of releasing the pins from the head of the pick and place device as instantly claimed, and in combination with the additional method steps.

Claim 24 is allowed because the prior art does not teach the step of removing the pins subsequent to passing at least one electrical signal between the semiconductor device package and the carrier substrate as instantly claimed, and in combination with the additional method steps.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT E...
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